IN THE CLAIMS

1. (Currently Amended)   A data transfer controller comprising:

an initial value register; and ~~(12, 13), a transfer start address of a transfer source or transfer destination being initially set to said initial value register from an external;~~ and

~~a control unit (3) which requests an interrupt to the external each time data transfer responding to a transfer request from the external reaches a predetermined data amount based upon the transfer start address, and initializes an address of the transfer source or transfer destination to the transfer start address in said initial value register each time the interrupt is issued a plurality of predetermined times.~~

a control unit,

wherein a transfer source address or a transfer destination address is initially set to said initial value register based upon an external request,

wherein said control unit starts data transferring operations based upon said external request, controls said

data transferring operations from said transfer source

address,

wherein said control unit issues an interrupt for each of

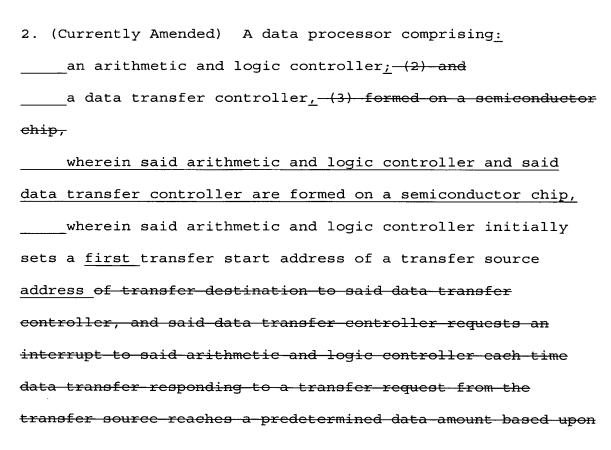predetermined data transferring operations, and

wherein said control unit initializes said transfer

destination address after said interrupt has been issued for a

predetermined plurality of times, and continues data

transferring operations to an initialized transfer destination

address without receiving an additional external request.

2. (Currently Amended) A data processor comprising:

an arithmetic and logic controller; (2) and

a data transfer controller, (3) formed on a semiconductor

chip,

wherein said arithmetic and logic controller and said

data transfer controller are formed on a semiconductor chip,

wherein said arithmetic and logic controller initially

sets a first transfer start address of a transfer source

address of transfer destination to said data transfer

controller, and said data transfer controller requests an

interrupt to said arithmetic and logic controller each time

data transfer responding to a transfer request from the

transfer source reaches a predetermined data amount based upon

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~~the transfer start address, and initializes an address of the~~

~~transfer source or transfer destination to the transfer start~~

~~address each time the interrupt is issued a plurality of~~

~~predetermined times.~~ and a second transfer start address of a

transfer destination address to said data transfer controller,

wherein said data transfer controller starts data

transferring based upon a transfer request from said

arithmetic and logic controller, and controls data

transferring from said transfer source address to said

transfer destination address and changes said transfer

destination address in response to data transferring,

wherein said data transfer controller issues an interrupt

to said arithmetic and logic controller each time a data

transfer request based upon a given transfer start address

reaches a predetermined data amount, and

wherein said data transfer controller changes said

transfer destination address to said second transfer start

address after said interrupt has been issued a predetermined

plurality of times, and restarts said data transferring to a

changed transfer destination address without receiving another

transfer request from said arithmetic and logic controller.

3. (Currently Amended) A data processing system comprising an arithmetic and logic controller ~~(2)~~, a data transfer controller ~~(3)~~ whose transfer control conditions are set by said arithmetic and logic controller, ~~a RAM (8) accessible by said arithmetic and logic controller and said data transfer controller,~~ and a peripheral circuit ~~(9)~~ which issues a transfer request to said data transfer controller, ~~wherein:~~

~~said data transfer controller requests an interrupt to said arithmetic and logic controller each time data transfer to said RAM responding to a transfer request from the said peripheral circuit reaches a predetermined data amount based upon a transfer start address of said RAM indicated by the transfer control conditions set by said arithmetic and logic controller, and initializes an address of the transfer source or transfer destination to the transfer start address each time the interrupt is issued a plurality of predetermined times; and~~

~~after the interrupt from said data transfer controller is acknowledged, said arithmetic and logic controller reads data transferred to said RAM before the interrupt is issued, and performs data processing.~~

<u>wherein said transfer control conditions includes a transfer source address and a transfer destination address,</u>

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wherein said data transfer controller starts data transferring based upon said transfer request from said peripheral circuit, controls data transferring from said transfer source address to said transfer destination address and changes said transfer destination address in response to data transferring,

wherein said data transfer controller issues an interrupt to the arithmetic and logic unit each time a data transfer request based upon a given transfer start address reaches a predetermined data amount,

wherein said data transfer controller initializes said transfer destination address after said interrupt has been issued a predetermined plurality of times, and continues said data transferring to said initialized transfer destination address without any additional request from said peripheral circuit or said arithmetic and logic controller.

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4. (Currently Amended) A data transfer controller comprising:

an initial ~~value~~ address register ~~(12, 13)~~ capable of being externally set with an initial transfer control address information as a first transfer control address information;

an address ~~counting~~ generating unit ~~(14, 15, 16)~~ which renews the first transfer control address information each

time data is transferred from a transfer source to a transfer

destination;

a temporary address register ~~(21) to which the~~ is set to

the first transfer control address information ~~set to said~~

~~initial value register is set, the set transfer control~~

~~address information being sequentially renewed by said address~~

~~counting means~~ as a second transfer control address

information, and this second transfer control address

information is renewed therein by said address generating

unit;

a transfer number counting unit ~~(14, 15, 16)~~ capable of

repetitively performing an operation of counting the number of

transfer times up to a first target number each time data is

transferred from the transfer source to the transfer

destination;

a repetition number counting unit ~~(20, 21, 22)~~ capable of

repetitively performing an operation of counting the number of

repetition times of the operation of said transfer number

counting unit which counts the number of transfer times up to

the first target number, up to a second target number; and

a control unit ~~(26)~~ which starts a data transfer

operation from the transfer source to the transfer destination

in response to a data transfer request, output~~ting~~s an

interrupt signal each time said transfer number counting unit

counts up to the first target number, and setsting the first

transfer control address information to said temporary

register from said initial value address register each time

said repetition number counting unit counts up to the second

target number.

5. (Currently Amended) A data transfer controller according

to claim 4, wherein:

wherein said temporary address register is a destination

address register for storing a transfer destination address,

wherein said initial value register is an initial address

register to which a start address of the transfer destination

is set, and

wherein said control unit is capable of starting a data

transfer control of storing data at the a transfer source

address in to the transfer destination at a transfer

destination address in the destination address register, in

response to the data transfer request.

6. (Currently Amended) A data transfer controller according

to claim 4, wherein:

wherein said temporary address register is a source address register for storing a transfer source address~,~

wherein said initial value register is an initial address register to which a start address of the transfer source is set~,~ and

wherein said control unit is capable of starting a data transfer control of storing data at the transfer source address in the source address register ~in~ to the transfer destination at a transfer destination address, in response to the data transfer request.

7. (Currently Amended) A data transfer controller according to claim 4, further comprising a source address register for storing a transfer source address and a destination register for storing a transfer destination address, ~wherein:~

wherein said control unit can select either said source address register or said destination address register as said temporary address register and can start a data transfer control by using ~the register selected as~ said temporary register, in response to the data transfer request.

8. (Currently Amended)   A data transfer controller according to ~any one of~ claim 4, further comprising a transfer number

designation register capable of being externally set with the first target number.

9. (Currently Amended) A data transfer controller according to ~~any one of~~ claim 4, wherein the second target number is three.

10. (Currently Amended) A data transfer controller according to ~~any one of~~ claim 1, further comprising a RAM usable as the transfer source or the transfer destination.

11. (Currently Amended) A data transfer controller, according to claim 4, further comprising a selecting circuit~~:~~,

wherein, said initial address register is capable of storing a plurality of said transfer control address information,

wherein said selecting circuit is capable of selecting an arbitrary one of said transfer control address information stored in said initial value register as said first transfer control address information

~~a plurality of initial value registers (12, 13) each capable of being externally set with transfer control address information;~~

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~~an address counting circuit (14, 15, 16) which renews~~
~~the transfer control address information each time data is~~
~~transferred from a transfer source to a transfer destination;~~
~~a selecting circuit (18) capable of selecting the~~
~~transfer control address information stored in one of a~~
~~plurality of said initial value registers;~~
~~a temporary address register (21) to which the transfer~~
~~control address information selected by said selecting circuit~~
~~is set, the set transfer control address information being~~
~~sequentially renewed by said address counting circuit;~~
~~transfer number counting circuit (14, 15, 16) capable of~~
~~repetitively performing an operation of counting the number of~~
~~transfer times up to a first target number each time data is~~
~~transferred from the transfer source to the transfer~~
~~destination;~~
~~a repetition number counting circuit (20, 21, 22) capable~~
~~of repetitively performing an operation of counting the number~~
~~of repetition times of the operation of said transfer number~~
~~counting circuit which counts the number of transfer times up~~
~~to the first target number, up to a second target number; and~~
~~a control circuit (26) which starts a data transfer~~
~~operation from the transfer source to the transfer destination~~
~~in response to a data transfer request, outputs an interrupt~~

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~~signal each time said transfer number counting means counts
the first target number, makes said selecting circuit select
said initial value register in accordance with a count of said
repetition number counting circuit, and sets the transfer
control address information in the selected initial register
to said temporary register~~.

12. (Currently Amended)   A data processor comprising an
arithmetic and logic controller ~~(2)~~ and a data transfer
controller according to claim 11, ~~(3) to which transfer control
conditions are set by said arithmetic and logic controller,
wherein said data transfer controller comprises:
an initial value register (12, 13) capable of being set
with transfer control address information by said arithmetic
and logic controller;
an address counting circuit (14, 15, 16) which renews the
transfer control address information each time data is
transferred from a transfer source to a transfer destination;
a temporary address register (21) to which the transfer
control address information set to said initial value register
is set, the set transfer control address information being
sequentially renewed by said address counting means;~~

~~a transfer number counting circuit (14, 15, 16) capable~~
~~of repetitively performing an operation of counting the number~~
~~of transfer times up to a first target number each time data~~
~~is transferred from the transfer source to the transfer~~
~~destination;~~

~~a repetition number counting circuit (20, 21, 22) capable~~
~~of repetitively performing an operation of counting the number~~
~~of repetition times of the operation of said transfer number~~
~~counting circuit for counting the number of transfer times up~~
~~to the first target number, up to a second target number; and~~

~~a control circuit (26) which starts a data transfer~~
~~operation from the transfer source to the transfer destination~~
~~in response to a data transfer request, outputs an interrupt~~
~~signal each time said transfer number counting circuit counts~~
~~the first target number, and sets the transfer control address~~
~~information in the initial register to said temporary register~~

<u>wherein said arithmetic and logic controller is capable
of set a transfer conditions to said initial address register
in said data transfer controller as said plurality of initial
transfer control address information, and is capable of
outputting said data transfer request to said data transfer
controller</u>.

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13. (Currently Amended) A data processor according to claim 12, further comprising a RAM accessible by said arithmetic and logic controller and said data transfer controller,

wherein said arithmetic and logic controller, said data transfer controller and said RAM are~~being~~ formed in a single semiconductor chip.

14. (Currently Amended) A data processor according to claim 13, further comprising a peripheral input/output circuit accessible by said arithmetic and logic controller and said data transfer controller,

wherein said peripheral input/output circuit is~~being~~ capable of outputting the data transfer request to said data transfer controller.

15. (Currently Amended) A data processing system comprising:

a data processor recited in claim 14; and

~~and~~ a voice signal input circuit ~~(41, 42)~~ connected to said peripheral input/output circuit of the data processor, ~~wherein:~~

wherein the data processor stores an operation program for said arithmetic and logic controller~~,~~,

wherein in accordance with the operation program, said arithmetic and logic controller sets transfer conditions to said data transfer controller, the transfer conditions being used when a voice signal input from said voice signal input circuit to said peripheral input/output circuit is transferred to said RAM,

wherein said data transfer controller controls to transfer the voice signal to said RAM in response to the data transfer request from said peripheral input/output circuit, and

wherein when an interrupt signal is received from said data transfer controller, said arithmetic and logic controller reads the voice signal from said RAM and processes the read voice signal.